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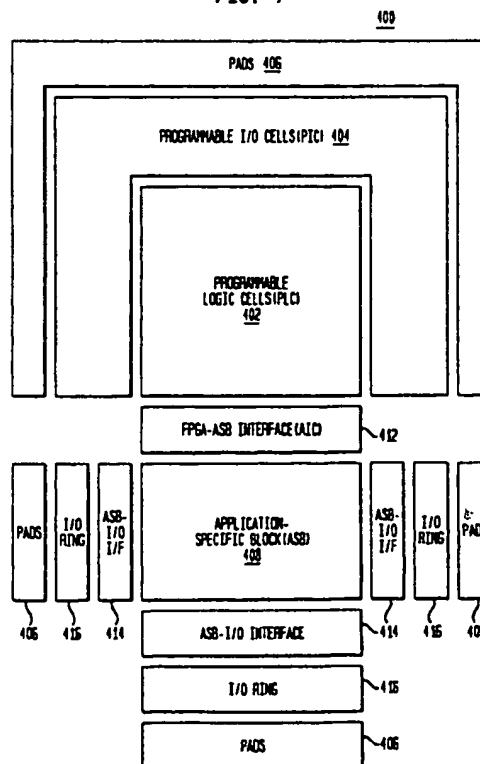
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### (54) Hybrid programmable gate arrays

(57) A single integrated circuit (IC) (400) having one or more regions of mask-programmed device (MPD) logic (408) for implementing permanent functions and one or more regions of field-programmable gate-array (FPGA) logic (402) for implementing user-specified functions. The FPGA-type logic provides programming flexibility, while the MPD-type logic provides size, speed, functionality, and dollar cost advantages. In one embodiment, a hybrid IC has an array of programmable logic cells (PLCs) (402) implemented using FPFA-type logic, an application-specific block (ASB) (408) implemented using MPD-type logic, and a ring of pads (406). Fast interface switch hierarchy (FISH) cells provide the interface between the PLC array and the pads, between the PLC array and the ASB, and between the ASB and the pad ring. Muxes in the FISH cells can be programmed to cause the FISH cells to operate either (1) as programmable interface cells (PICs) that provide a direct interface between the PLC array and the pad ring or (2) as ASB-interface cells (AICs) that (a) provide interfaces between the PLC array and the ASB and (b) control interfaces between the ASB and the pad ring.

FIG. 4



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## Description

### Field of the Invention

[0001] The present invention relates to integrated circuits, and, in particular, to programmable gate arrays and application-specific integrated circuits.

### Description of the Related Art

[0002] Programmable gate arrays constitute one family of integrated circuits. There are different types of programmable gate arrays. A mask-programmable gate array (MPGA) (also known as a factory-programmable gate array) is a type of mask-programmed integrated circuit that is programmed one time and typically by the manufacturer of the gate array. Other types of mask-programmed devices (MPDs) include full-custom devices and standard-cell devices. A field-programmable gate array (FPGA), on the other hand, is a type of gate-array integrated circuit that can be programmed by the user. An FPGA can be one-time programmable or re-programmable, in which case the user can re-program the gate array one or more times.

[0003] Fig. 1 shows a schematic diagram of a conventional FPGA 100, having an array 102 of programmable logic cells (PLCs) surrounded by a ring 104 of programmable input/output (I/O) cells (PICs) and an outermost ring 106 of pads. The PLCs and PICs can be programmed (and possibly reprogrammed) in the field to implement a desired set of functions. This programming is typically done through the configuration interface of the FPGA, which reads a stream of bits and writes to the internal configuration storage (SRAM, EEPROM, anti-fuse, etc.), which in turn controls the programmable logic and routing. The PICs operate as the interfaces between the array of PLCs and individual pads, which provide connections to the "outside world," that is, circuitry external to the FPGA. Programmable general routing resources (not shown in Fig. 1) are used to implement specific connections between PLC array 102 and PIC ring 104 (i.e., PLC-PIC connections) as well as specific connections within PLC array 102 (i.e., PLC-PLC connections) and within PIC ring 104 (i.e., PIC-PIC connections).

[0004] Fig. 2 shows a detail of a portion of FPGA 100 of Fig. 1. According to one conventional design, each PIC in ring 104 is associated with four pads and has four corresponding sets of pad logic. Fig. 2 shows a schematic diagram of the circuitry of FPGA 100 that is associated with one of these sets of pad logic. PLC logic 202 and PLC local routing 204 are part of PLC array 102 of Fig. 1. Similarly, PIC local routing 208 and PIC logic 210 are part of PIC ring 104 of Fig. 1, while pad 212 is one of the pads of pad ring 106 of Fig. 1. General routing resources 206 correspond to the programmable routing and logic used to connect individual sets of PLC logic to individual sets of PIC logic. PIC logic 210 comprises an

output buffer 216 and an input buffer 218, as well as boundary scan and other miscellaneous PIC logic 214, such as optional flip-flops and latches.

[0005] Fig. 3 shows a schematic diagram of one of the three main types of mask-programmed devices -- a conventional MPGA 300, having an array of gates 302 surrounded by a ring of pads 306. Typically, the array of gates and the ring of pads are interconnected with each other by conductive (typically metal) wires to implement a desired set of functions. The ring of pads serves the same purpose of interfacing to the "outside world" as the ring of pads in FPGA 100 of Fig. 1. In a typical MPGA, the array of gates and the array of pads are pre-defined and the user can only define how they are interconnected at the factory. The other two main types of MPDs are standard-cell devices, which have rows of standard cells instead of an array of gates, and full-custom devices, which have individual transistors instead of an array of gates. These two types of devices also differ from MPGAs in that the rows of standard cells and the arrays of transistors are not pre-fixed, thus allowing increased functionality.

[0006] An FPGA, such as FPGA 100 of Fig. 1, has the flexibility to implement many different logic functions using the same silicon, although the cost of this flexibility is in chip layout area, performance (i.e., speed and power dissipation), and dollar cost. An MPGA could be designed to implement the same piece of logic with less area and optimal performance, translating into a lower dollar cost. The cost of using an MPGA, however, is that, once it is manufactured, the logic function cannot be changed by the user.

[0007] The present invention is directed to a scheme for exploiting both the programming flexibility advantages of FPGAs and the size, speed, functionality, and dollar cost advantages of MPDs.

### Summary of the Invention

[0008] In general, the present invention is directed to a single hybrid integrated circuit (IC) having one or more regions of MPD-type logic for implementing permanent functions and one or more regions of FPGA-type logic for implementing user-specified functions. The FPGA-type logic provides programming flexibility, while the MPD-type logic provides size, speed, functionality, and dollar cost advantages. In one embodiment, a hybrid IC has an array of programmable logic cells (PLCs) implemented using FPGA-type logic, an application-specific block (ASB) implemented using MPD-type logic, and a ring of pads. Fast interface switch hierarchy (FISH) cells provide the interface between the PLC array and the ASB. Muxes in the FISH cells can be programmed to cause the FISH cells to operate either (1) as programmable interface cells (PICs) that provide a direct interface between the PLC array and the pad ring or (2) as ASB-interface cells (AICs) that provide interfaces between the PLC array and the ASB.

[0009] Another aspect of the invention is the ability to program the FPGA portion of the hybrid device separate from the ASB portion. The invention also includes the ability to modify the logic functionality in the ASB portion by setting options in the FPGA portion.

#### **Brief Description of the Drawings**

[0010] Other aspects, features, and advantages of the present invention will become more fully apparent from the following detailed description, the appended claims, and the accompanying drawings in which:

Fig. 1 shows a schematic diagram of a conventional FPGA;

Fig. 2 shows a detail of a portion of the conventional FPGA of Fig. 1 ;

Fig. 3 shows a schematic diagram of a conventional MPGA;

Fig. 4 shows a schematic diagram of a hybrid integrated circuit, according to one embodiment of the present invention; and

Fig. 5 shows a schematic diagram of the circuitry of the hybrid IC of Fig. 4 that is associated with one set of FISH-cell logic, according to one embodiment of the present invention.

#### **Detailed Description**

[0011] Depending on the type or types of applications for which a conventional FPGA is to be used, there may be certain functions that many users will want to program into their FPGAs. Such functions may include anything that, in the past, has been placed in an MPD. According to the present invention, this permanent functionality can be implemented in MPD-type logic, while other user-specified functionality is implemented in FPGA-type logic, all on the same chip.

[0012] The present invention is directed to hybrid circuitry that combines one or more regions of FPGA-type logic with one or more regions of MPD-type logic on a single integrated circuit (IC) chip. By combining both FPGA- and MPD-type logic on one die, the advantages of both may be reaped. A specific logic function that requires high performance and/or needs to be very dense and/or is not possible in an FPGA (e.g., implementing an analog circuit with critical characteristics) can be implemented in MPD-type logic on a die with FPGA-type logic around it. The invention permits changes to functionality, when needed, yet provides improved performance and smaller device size over conventional FPGAs.

[0013] In particular, the regions of MPD-type logic may be pre-programmed in the factory to implement functions that, with conventional FPGAs, would be programmed in the field. The regions of FPGA-type logic are then left for the user to program in the field. In this way, a hybrid IC of the present invention combines the programming flexibility of FPGA-type logic with the size

and speed advantages of MPD-type logic. As a result, the hybrid IC can have faster speed, smaller area, and lower dollar cost than conventional FPGAs which have only FPGA-type logic, without losing the flexibility of field programming that give FPGAs an advantage over conventional MPDs. This allows applications to be split into two categories of functions: permanent functions and user-specified functions. According to the present invention, permanent functions can be implemented in MPD-type logic for fast speed, small area, and low power usage, while the user-specified functions are implemented in FPGA-type logic.

[0014] Fig. 4 shows a schematic diagram of a hybrid integrated circuit 400, according to one embodiment of the present invention. Similar to conventional FPGA 100 of Fig. 1, hybrid IC 400 comprises an array 402 of programmable logic cells surrounded on three sides by a ring of programmable I/O cells 404 and an outermost ring of pads 406. On its fourth side, however, PLC array 402 is bounded by sets of FPGA-ASB interface hardware 412 that allow PLC array 402 to interface with an application specific block (ASB) 408, which is implemented using MPD-type logic. For purposes of this specification, each set of FPGA-ASB interface hardware is referred to as an ASB-interface cell (AIC).

[0015] In a preferred embodiment, the PICs and AICs are implemented using the same generic set of field-programmable logic and routing circuitry, which is programmed to function as either a PIC or an AIC. For purposes of this specification, this generic set of programmable logic and routing circuitry is referred to as a fast interface switch hierarchy (FISH) cell. Each FISH cell is preferably programmed in the factory to function either (1) as a PIC that forms an interface between PLC array 402 and the corresponding pads 406 or (2) as an AIC that forms interfaces between PLC array 402 and ASB 408.

[0016] A FISH cell can be programmed in the factory or in the field to function as a PIC or as an AIC. Even when programmed in the factory, there are other aspects of a programmed FISH cell that are still field programmable. That is, when factory-programmed to function as a PIC, a FISH cell has the same field programmability of a conventional PIC, such as those used in conventional FPGA 100 of Fig. 1. Similarly, when factory-programmed to function as an AIC, a FISH cell has other field programmable aspects.

[0017] Fig. 5 shows a schematic diagram of the circuitry of hybrid IC 400 of Fig. 4 that is associated with one set of FISH-cell logic, when operating as an AIC, according to one embodiment of the present invention. PLC logic 502 and PLC local routing 504 are part of PLC array 402 of Fig. 4. General routing resources 506 correspond to the programmable routing and logic used to connect individual sets of PLC logic to individual sets of FISH-cell logic and any other logic blocks. Pad 512, output buffer 516, and input buffer 518 are analogous to pad 212, output buffer 216, and input buffer 218 of Fig.

2, respectively. Also, the optional boundary scan and miscellaneous logic 214 of Fig. 2 is broken into logic 514a and 514b of Fig. 5.

[0018] For this particular implementation, the FISH-cell of Fig. 5, according to the present invention, differs from the conventional PIC circuitry of Fig. 2 in a number of significant ways. First of all, the ASB block 520 includes mux 534, which is used to select between signal 540 from FISH cell 508 or signal 542 from ASB logic 528, to be sent to output buffer 516 through optional boundary scan block 514a. This selection can be set by configuration RAM cell 524 in FISH cell 508, whose output is tied to the control input of mux 534. Optionally, signal 540 from FISH cell 508 can also be sent to ASB logic 528. Another option would be to permanently tie the control lead to mux 534 at the factory, thus permanently selecting one of the signals to be sent to output buffer 516. In the same manner, signals from the input buffer 518 can be sent to ASB logic 528 and/or to FISH cell 508 after passing through optional boundary scan block 514a. Mux 532, whose control lead is driven by the output of RAM cell 522, is used to select either output signal 546 from ASB logic 528 or the signal from input buffer 518, to be sent to FISH cell 508 through signal 544. Optionally, the control lead to mux 532 could again be permanently tied.

[0019] Another significant difference between the FISH-cell circuitry of Fig. 5 and the conventional PIC circuitry of Fig. 2 is the addition of one or more extra programmable RAMs and/or other programming elements (526) within FISH cell 508. FISH cell 508 and ASB logic 528 can use these memory cells to provide a limited amount of flexibility in the ASB.

[0020] In order for the FISH-cell circuitry of Fig. 5 to function as a conventional PIC, muxes 532 and 534 may be programmed to provide direct connections between boundary scan logic 514a and other miscellaneous FISH-cell logic 514b. On the other hand, in order for the FISH-cell circuitry of Fig. 5 to function as an ASB-interface cell, muxes 532 and 534 may be programmed to provide (1) connections between PLC logic 502 and ASB 520, and (2) connections between ASB 520 and pad 512 via I/O logic 516 and 518.

[0021] As mentioned previously, each FISH cell is both mask programmable and field programmable. It is optionally mask programmable in the factory to allow certain connections that dictate whether or not the FISH cell will be interfacing to an ASB or I/O logic, that is, whether the FISH cell will function as an AIC or a PIC. Whether or not a FISH cell is programmed to interface to an ASB, in one preferred embodiment, the FISH cell still looks like a PIC at the edge of the PLC array, thereby keeping the PLC-PIC boundary consistent around the chip. This alleviates any software issues involved in placing an ASB within an FPGA, because the PLC-PIC array connections are essentially unchanged. Although the chip size may change when an ASB is incorporated on an FPGA, the PLC array itself will not have to have

a different architectural model. Timing models will also remain the same for the PLC array with or without an ASB. The FISH cell may be mask programmed in the factory to adjust the load on certain global signal distribution networks so as to keep the timing models the same.

[0022] One advantage of using a single generic FISH-cell design of Fig. 5 for both the PICs and the AICs of a hybrid IC of the present invention is that the hybrid IC will work with existing FPGA software tools that are used for conventional FPGAs, such as FPGA 100 of Fig. 1. In an IC having only FPGA-type logic and no ASB, each FISH cell will be mask programmed to operate as a PIC. As such, the generic FISH cell of Fig. 5 can be used in any FPGA-related circuit -- either those ICs having only FPGA-type logic or those hybrid ICs having both FPGA- and MPD-type logic.

[0023] Depending on the embodiment, the FPGA-type logic in a hybrid IC of the present invention may be implemented using any suitable type of field-programmable logic, such as SRAM-based, DRAM-based, fuse-programmable, anti-fuse-programmable, EPROM-based, or EEPROM-based gate-array logic. Similarly, the MPD-type logic may be implemented using any suitable type of mask-programmable logic, such as nMOS, pMOS, CMOS, GaAs, etc.

[0024] Programming of the FPGA-type logic is typically done through a configuration interface that reads a stream of bits and writes data into the configuration storage, which then controls the programmable logic and routing. Typically, this configuration interface can read this stream of data automatically from many external storage media, including serial PROMs, parallel PROMs, and by interfacing with a microprocessor. One embodiment of Fig. 4 allows ASB block 408 to interface with the configuration interface logic directly, thus allowing the ASB logic to write the configuration bits, as well as control the configuration process and receive the status of the configuration process.

[0025] In the embodiment of Fig. 4, hybrid IC 400 has one region of FPGA-type logic (i.e., PLC array 402) and one region of MPD-type logic (i.e., ASB 408). In general, the present invention can be implemented as a single IC having one or more regions of FPGA-type logic and one or more regions of MPD-type logic. Moreover, the type of logic used may differ from region to region. For example, a first region of FPGA-type logic may be implemented using SRAM-based gate-array logic, while a second region of FPGA-type logic of the same hybrid IC may be implemented using DRAM-based gate-array logic. Similarly, a hybrid IC of the present invention could have regions implemented using two different types of MPD-type logic.

[0026] It will be further understood that various changes in the details, materials, and arrangements of the parts which have been described and illustrated in order to explain the nature of this invention may be made by those skilled in the art without departing from the prin-

ciple and scope of the invention as expressed in the following claims.

# Claims

1. An integrated circuit (IC) comprising one or more regions of FPGA-type logic and one or more regions of MPD-type logic.
2. The invention of claim 1, wherein the FPGA-type logic contains programming elements that are one of SRAM-based logic, DRAM-based logic, fuse-programmable logic, anti-fuse-programmable logic, EPROM-based logic, and EEPROM-based gate-array logic and the MPD-type logic is one of mask-programmed gate array logic, standard-cell logic, and full-custom logic.
3. The invention of claim 1, wherein the IC comprises more than two different types of FPGA-type logic or MPD-type logic.
4. The invention of claim 3, wherein the IC comprises one or more regions of a first type of FPGA-type logic, one or more regions of a second type of FPGA-type logic, and one or more regions of MPD-type logic.
5. The invention of claim 3, wherein the IC comprises one or more regions of a first type of MPD-type logic, one or more regions of a second type of MPD-type logic, and one or more regions of FPGA-type logic.
6. The invention of claim 1, wherein the IC comprises flexible interface logic adapted to be programmed to operate either (1) as an input/output (I/O) cell for direct connection between a region of FPGA-type logic and a pad or (2) as an interface (I/F) cell for connections between a region of FPGA-type logic and a region of MPD-type logic.
7. The invention of claim 6, wherein the flexible interface logic is mask programmable to operate either as an I/O cell or as an I/F cell.
8. The invention of claim 6, wherein the flexible interface logic comprises a set of muxes that are programmable to provide either (1) the direct connections between the region of FPGA-type logic and the pad or (2) the connections between the region of FPGA-type logic and the region of MPD-type logic.
9. The invention of claim 8, wherein the set of muxes separates boundary scan logic from other miscellaneous logic.
10. The invention of claim 6, wherein the flexible interface logic comprises programmable RAMs or other programming elements adapted to be used by the MPD-type logic.
11. The invention of claim 6, wherein programmable RAMs or other programming elements in the flexible interface logic are adapted to control connections between the MPD-type logic and a pad.
12. The invention of claim 1, wherein the MPD-type logic is pre-programmed to implement functions that are generally field programmed into ICs having only FPGA-type logic.
13. The invention of claim 1, wherein the MPD-type logic is pre-programmed to implement functions that are not possible in ICs having only FPGA-type logic.
14. The invention of claim 1, wherein configuration data, configuration process control, and configuration process status used to program the FPGA-type logic is provided by an interface between the FPGA-type logic and the MPD-type logic.
15. An integrated circuit comprising:
  - (a) an array of programmable logic cells (PLCs);
  - (b) an application-specific block (ASB);
  - (c) a ring of pads; and
  - (d) a ring of fast interface switch hierarchy (FISH) cells providing an interface between the PLC array and the ASB.
16. The invention of claim 15, wherein the PLC array is implemented using FPGA-type logic and the ASB is implemented using MPD-type logic.
17. The invention of claim 15, wherein each FISH cell is adapted to be programmed to function (i) as a programmable input/output cell (PIC) to provide a direct interface between the PLC array and the pad ring or (ii) as an ASB-interface cell (AIC) to provide an interface between the PLC array and the ASB.
18. The invention of claim 17, wherein each FISH cell contains logic to control connections between the ASB and the pad ring.
19. The invention of claim 15, wherein each FISH cell is mask programmable.
20. The invention of claim 15, wherein each FISH cell comprises:
  - (1) local routing resources;
  - (2) boundary scan logic adapted to be connect-

ed to the local routing resources;  
(3) other miscellaneous logic;  
(4) interface logic separating the boundary scan logic and the other miscellaneous logic;  
and  
(5) input/output logic, comprising at least one of an input buffer and an output buffer, and adapted to be connected to the other miscellaneous logic and a pad of the pad ring.

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21. The invention of claim 20, wherein the interface logic comprises muxes that are adapted to be programmed to determine whether the FISH cell operates as a PIC or as an AIC.

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22. The invention of claim 20, wherein the FISH cell comprises programmable RAMs or other programming elements adapted to be used by the ASB.

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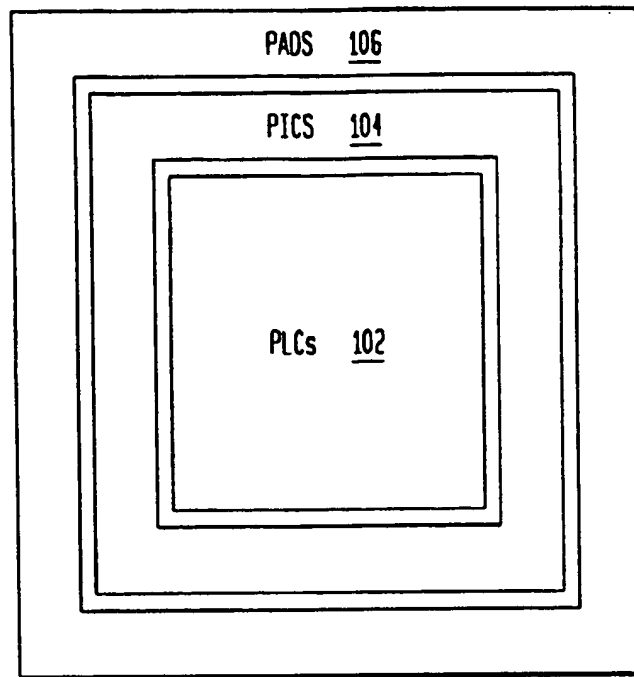
45

50

55

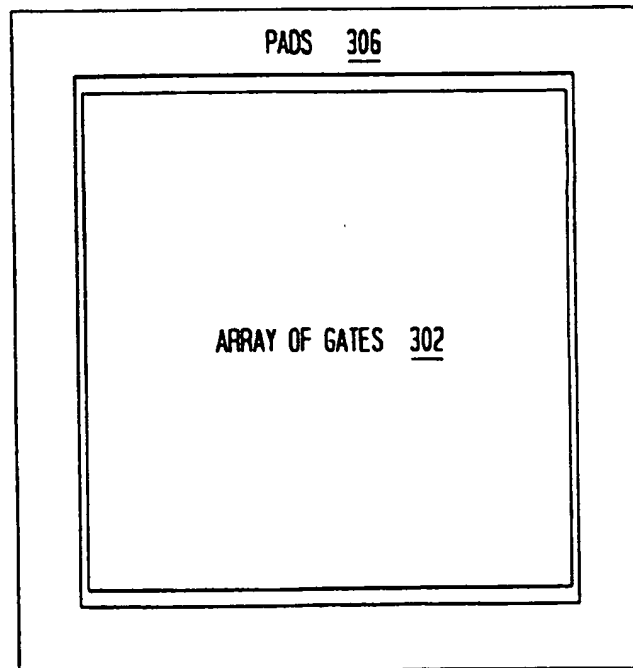
**FIG. 1**  
(PRIOR ART)

100



**FIG. 3**  
(PRIOR ART)

300



**FIG. 2**  
(PRIOR ART)

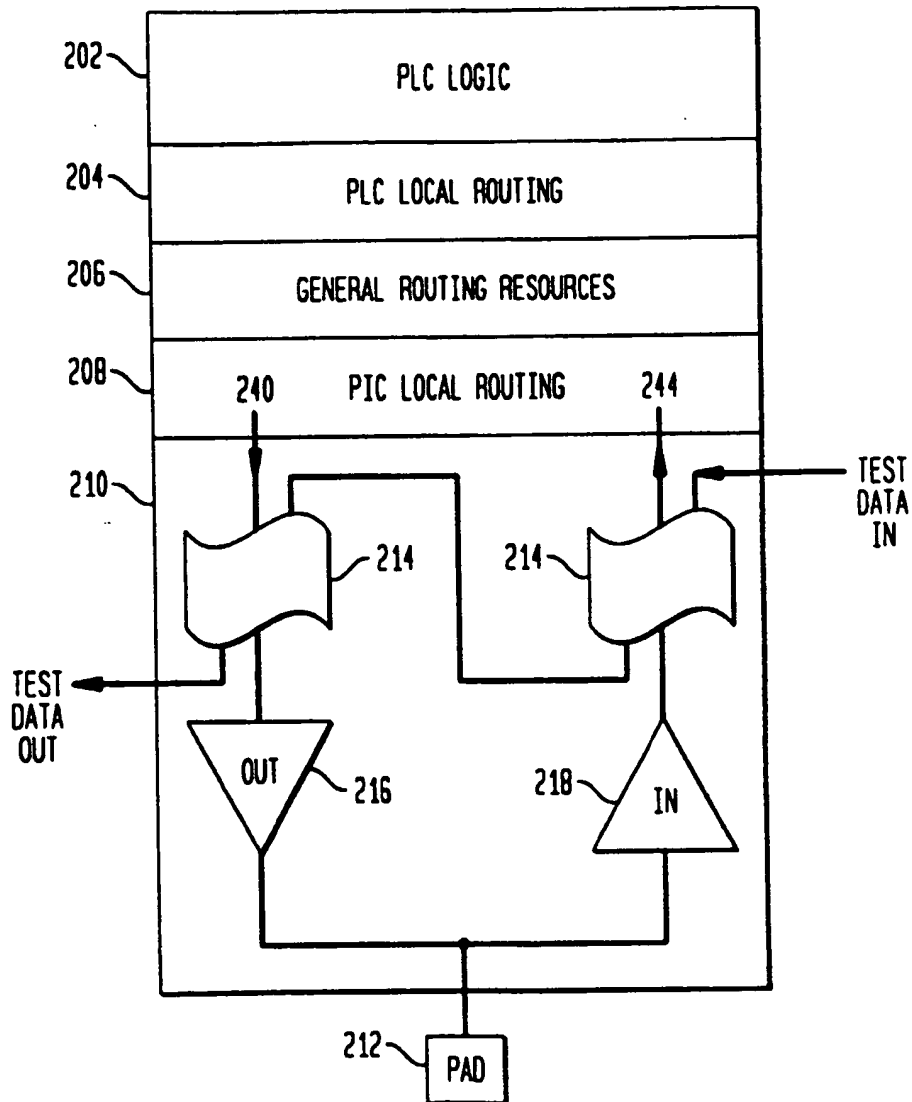




FIG. 4

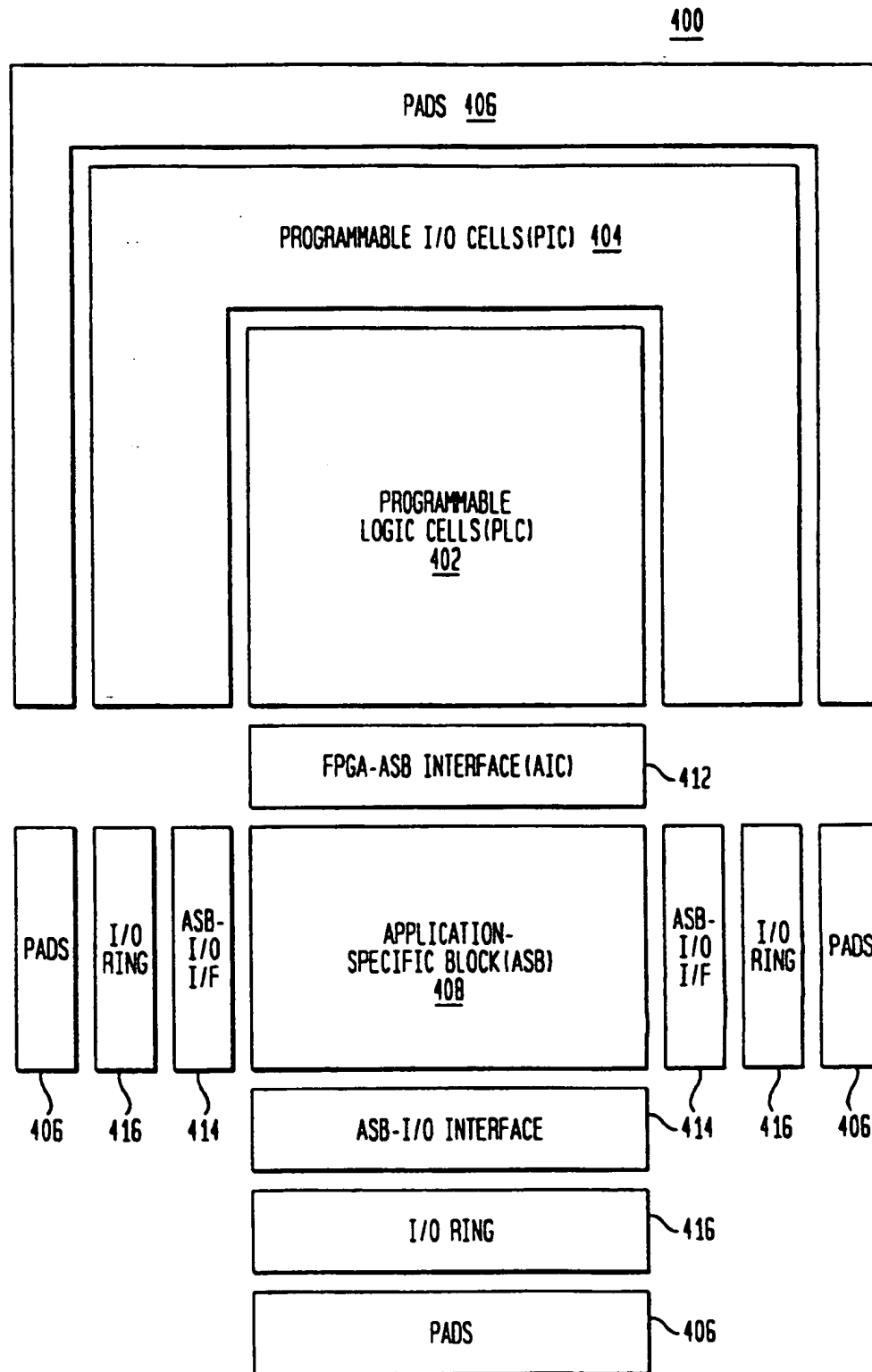


FIG. 5

